~~Attorney Docket No. TI-35444 (1962-05414)~~; "Micro-Sequence Execution In A Processor," Serial No. 10/632,216, filed July 31, 2003~~, Attorney Docket No. TI-35445 (1962-05415)~~; "Program Counter Adjustment Based On The Detection Of An Instruction Prefix," Serial No. 10/632,222, filed July 31, 2003~~, Attorney Docket No. TI-35452 (1962-05416)~~; "Reformat Logic To Translate Between A Virtual Address And A Compressed Physical Address," Serial No. 10/632,215, filed July 31, 2003~~, Attorney Docket No. TI-35460 (1962-05417)~~; "Synchronization Of Processor States," Serial No. 10/632,024, filed July 31, 2003~~, Attorney Docket No. TI-35461 (1962-05418)~~; "Conditional Garbage Based On Monitoring To Improve Real Time Performance," Serial No. 10/631,195, filed July 31, 2003~~, Attorney Docket No. TI-35485 (1962-05419)~~; "Inter-Processor Control," Serial No. 10/631,120, filed July 31, 2003~~, Attorney Docket No. TI-35486 (1962-05420)~~; "Cache Coherency In A Multi-Processor System," Serial No. 10/632,229, filed July 31, 2003~~, Attorney Docket No. TI-35637 (1962-05421)~~; and ~~"Concurrent Task Execution In A Multi-Processor, Single Operating System Environment," Serial No. 10/632,077, filed July 31, 2003, Attorney Docket No. TI-35638 (1962-05422).~~ "A Multi-Processor Computing System Having A Java Stack Machine And A RISC-Based Processor," Ser. No. 10/631,939, filed July 31, 2003.

Please replace paragraph [0037] with the following amended paragraph:

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[0037] In at least some embodiments of the invention, the MPU **104** may prioritize multiple tasks when awake. For example, if the MPU **104** has been awoken by a system interrupt **209**, more than one interrupt source may have positioned the system interrupt **209** and the MPU **104** will perform the associated tasks according to their pre-determined priority. In at least some embodiments, an operating system ("O/S") running ~~of~~ on the MPU **104** may control the order in which the MPU **104** carries out multiple interrupt requests.

Please replace paragraph [0039] with the following amended paragraph:

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[0039] In embodiments in which multiple signals (e.g. system interrupt **209**, system interrupt detect **216**, wait release **214**) occur simultaneously, approximately simultaneously, or concurrently, the operating system ("O/S") running on the MPU **104** may decide, according to a pre-determined priority, whether the MPU **104** will execute instructions as requested by the JSM **102** or execute the task(s) requested by the system interrupt **209**. As shown in ~~FIG. 6~~ **FIG. 3**,